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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/987,271	11/14/2001	Kenji Fukuda	216111US2X	6952

22850 7590 04/12/2002

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EXAMINER
NGUYEN, JOSEPH H

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/987,271	Applicant(s) KENJI FUKUDA	
	Examiner Joseph Nguyen	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11, 17-21, 39-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pfiester in view of Ohno et al.

Regarding claims 1-6, Pfiester discloses on figure 6 substantially all the structure set forth in the claimed invention except the silicon carbide region. However, Ohno discloses on figure 1 the silicon carbide region. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Pfiester by having the silicon carbide region for the purpose of obtaining a larger dielectric breakdown strength as taught by Ohno (col. 1, lines 36-37).

Regarding claim 7, Pfiester discloses on figure 6 the buried channel region 48 contains a diffusion of phosphorus at a maximum concentration that is from $5X10^{15}$ cm^{-3} to $1X10^{18}$ cm^{-3}. (col. 6, line 68).

Regarding claims 8 and 9, Pfiester discloses on figure 6 between the buried channel region 48 and the source and drain regions 28, 30 there is a region 22 having an impurity concentration that is not lower than a maximum impurity concentration of the impurity region used to form the buried channel region and not higher than an impurity concentration of the source or drain regions.

Regarding claims 10 and 11, Pfiester discloses on figure 6 between the buried channel region and the source and drain regions there is a diffusion layer of arsenic at a maximum concentration that is from $5X10^{16}$ cm^{-3} to $1X10^{19}$ cm^{-3}. (col. 7, lines 1-2).

Regarding claims 39 and 40, Pfiester discloses the gate electrode if formed of aluminum or an alloy that contains aluminum.

Regarding claims 17-21, Pfiester discloses on figure 6 substantially all the structure set forth in the claimed invention except the device formed on a (11-20) surface or a (000-1) surface of a hexagonal system or rhombohedral system or a (110) surface of a cubic system carbide crystal. However, Ohno discloses on figure 1 the device formed on a (11-20) surface or a (000-1) surface of a hexagonal system or rhombohedral system or a (110) surface of a cubic system carbide crystal. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Pfiester by having the device formed on a (11-20) surface or a (000-1) surface of a hexagonal system or rhombohedral system or a (110) surface of a cubic system carbide crystal for the purpose of decreasing the leakage current in a field effect transistor (See Abstract of Ohno et al).

Claims 1,2, 7, 12, 22 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Christie et al in view of Ohno.

Regarding claims 1 and 2, Christie et al discloses on figure 1 substantially all the structure set forth in the claimed invention except the silicon carbide region. However,

Ohno discloses on figure 1 the silicon carbide region. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Christie et al by having the silicon carbide region for the purpose of obtaining a larger dielectric breakdown strength as taught by Ohno (col. 1, lines 36-37).

Regarding claim 7, Christie et al discloses on figure 1 the buried channel region 20 contains a diffusion of arsenic at a maximum concentration that is from $5X10^{15}$ cm^{-3} to $1X10^{18}$ cm^{-3}.

Regarding claim 12, Christie et al discloses on figure 1 there is a P type impurity diffusion region 22 having an impurity concentration that is higher than an impurity concentration of the semiconductor substrate 12, said p type impurity diffusion region being located adjacently under the buried channel region 20.

Regarding claim 22, Christie et al discloses on figure 1 substantially all the structure set forth in the claimed invention except the device formed on a (11-20) surface or a (000-1) surface of a hexagonal system or rhombohedral system or a (110) surface of a cubic system carbide crystal. However, Ohno discloses on figure 1 the device formed on a (11-20) surface or a (000-1) surface of a hexagonal system or rhombohedral system or a (110) surface of a cubic system carbide crystal. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Christie et al by having the device formed on a (11-20) surface or a (000-1) surface of a hexagonal system or rhombohedral system or a (110) surface of a cubic system carbide crystal for the purpose of decreasing the leakage current in a field effect transistor (See Abstract of Ohno et al).

Regarding claim 41, Christie et al discloses on figure 1 the gate electrode 28 is formed of aluminum (col. 2, line 54).

Claims 13-16, 23 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pfiester and Ohno as applied to claim 10 above, and further in view of Christie et al.

Regarding claims 13-14, Pfiester and Ohno disclose substantially all the structure set forth in the claimed invention except a P type impurity diffusion region having an impurity concentration that is higher than an impurity concentration of the semiconductor substrate, said P type impurity diffusion region being located adjacently under the buried channel region. However, Christie et al discloses on figure 1 a P type impurity diffusion region 22 having an impurity concentration that is higher than an impurity concentration of the semiconductor substrate 12, said P type impurity diffusion region being located adjacently under the buried channel region 20. In view if such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Pfiester and Ohno by having a P type impurity diffusion region having an impurity concentration that is higher than an impurity concentration of the semiconductor substrate, said P type impurity diffusion region being located adjacently under the buried channel region for the purpose of improving the operation of an MIS transistor.

Regarding claims 15-16, 23 and 42, Pfiester and Ohno and Christie et al disclose the structure set forth in claims 15-16, 23 and 42.

Claims 24-28, 30-34 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pfiester and Ohno as applied to claim 2 above, and further in view of Bulucea et al.

Regarding claims 24-28, 30-34 and 38, Pfiester and Ohno disclose substantially all the structure set forth in the claimed invention except the device having a lateral resurf or lateral DMOS type MOSFET structure. However, Bulucea et al discloses the device having a lateral resurf or lateral DMOS type MOSFET structure. In view of such teaching, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Pfiester and Ohno by having the device having a lateral resurf or lateral DMOS type MOSFET structure for the purpose of effectively implementing the device into the memory cell device.

Claims 29, 32, 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Christie et al and Ohno as applied to claim 12 above, and further in view of Bulucea et al.

Regarding claims 29, 32, 35-37, Christie et al and Ohno disclose substantially all the structure set forth in the claimed invention except the device having a lateral resurf or lateral DMOS type MOSFET structure. However, Bulucea et al discloses the device having a lateral resurf or lateral DMOS type MOSFET structure. In view of such teaching, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Christie et al and Ohno by having the device having a

lateral resurf or lateral DMOS type MOSFET structure for the purpose of effectively implementing the device into the memory cell device.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent 5814869 to Dennen discloses a Femi threshold field effect transistor.

US Patent 6114728 to Yamazaki et al discloses the fabrication of a MIS semiconductor device of high reliability.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (703) 308-1269. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 308-7382 for regular communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JN
April 5, 2002

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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